Amendments to the Specification

Please replace the paragraph at page 15, line 28 – page 16, line 18 with the following amended paragraph:

Also, the buffer circuits 301a to 301c, 302a to 302c, 303a to 303c, 304a to 304c for shaping the signal waveform are arranged midway of the signal path group 111. Even in the case where the main circuit block CB0 and the subsidiary circuit block CBi are distant from each other and the wiring conductors of the signal path group 111 are long with a large time constant, therefore, the transmission time required for the signal to arrive at the receiving end from the transmitting end can be reduced as compared with ~~the the~~ the case in which the buffer circuits are absent. Further, in the case where the data of a plurality of bits are transmitted in parallel, the transmission variations between the bits can be suppressed. At the same time, the circuit block at the transmitting end can transmit a signal before the preceding signal previously transmitted reaches the circuit block at the receiving end. This system configuration can shorten the time required for transmitting continuous data.

Please replace the paragraph at page 21, lines 9-20 with the following amended paragraph:

The blocks PB1 to PB4 and ~~CB1 to CB4~~ CB1A to CB4A include interface circuits I/F 11A to I/F 14A and I/F 81 to I/F 84, respectively, for transmitting and receiving signals to and from the blocks. In this embodiment, the interface circuits I/F 11A to I/F 14A of the main circuit block PB1 are connected to the interface

circuits I/F 51, I/F 62, I/F 72, I/F 81 of the subsidiary circuit blocks CB1 to CB4 by the signal path groups 111a, 111b, 114a, 114b, 112a, 112b, 113a, 113b. Of these signal path groups, the signal path groups 111b to ~~1114b~~ 114b each include a signal path for transmitting the clock in parallel.

Please replace the paragraph at page 21, line 21 – page 22, line 9 with the following amended paragraph:

Though not shown in Fig. 5, the interface circuits I/F 21A to I/F 24A of the main circuit block PB2 and the interface circuits I/F 52, I/F 61, I/F 71, I/F 82 of the subsidiary circuit blocks ~~CB1 to CB4~~ CB1A to CB4A are also connected to each other by similar signal path groups. These signal path groups also each include a signal path for transmitting the clock in parallel. This is also the case with the main circuit blocks PB3, PB4. According to this embodiment, the subsidiary circuit blocks ~~CB1 to CB4~~ CB1A to CB4A each include a PLL circuit 120 and are each configured to generate an internal clock based on a clock signal CLK supplied from an external source. A part or all of the subsidiary circuit blocks ~~CB1 to CB4~~CB1A to CB4A, like in the embodiment shown in Fig. 1, can be configured so that the clock transmitted in parallel from the main circuit blocks PB1 to PB4 is used as an internal clock.

Please replace the paragraph at page 22, lines 10-14 with the following amended paragraph:

Fig. 6 shows in detail a section for transmitting/receiving the signal between a

given one of the main circuit blocks PB1 to PB4 and a given one of the subsidiary circuit blocks ~~CB1 to CB4~~ CB1A to CB4A shown in Fig. 5.

Please replace the paragraph at page 24, line 21 – page 25, line 13 with the following amended paragraph:

Numeral 470 designates a phase regulating circuit for regulating the phase by delaying the clock Dckpt received by the buffer 493, and numerals 451 to 454 latch circuits for receiving and sequentially shifting the sync signal Synct received by the buffer 492, based on the clock Dckptd which is phase-regulated by the phase regulating circuit 470. Numeral 455 designates a distribution circuit for distributing the signal latched by the latch circuits 451 to 454 and the clock Dckpt_d phase-regulated by the phase regulating circuit 470, to the input latch circuits 444 to 447 as a clock Dckpt_d, together with the enable signal ~~CKEN0~~ CKEN0 to CKEN3. Out of the signals output from the distribution line pattern wiring network 455, the clock Dckpt_d is fed back to the phase regulating circuit 470, which in turn compares the phase of the clock Dckpt_d fed back with the phase of the receiving clock Dckpt and regulates the two phases to be coincident with each other. Character Dckpt_d designates a clock generated by distribution of Dckpt_out in the distributing circuit 455.

Please replace the paragraph at page 32, line 20 – page 33, line 11 with the following amended paragraph:

The clock Thcycd output from the variable delay circuit 474A1 is supplied to the second DLL circuit 470B and compared with the phase of the clock signal Dckpt_d distributed to the input latch circuits 444 to 447. Thus, the output clock Dckpt_out is generated with the phase difference of zero (see Figs. 11(c) to (e)). As a result, even in the case where the number of bits of the data transmitted increases and the input latch circuits ~~444 to 44y~~ 444 to 447 are increased with an increased clock supply wiring conductor length so that the delay of the clock signal Dckpt_d distributed increases to an extent not negligible, the leading edge and the trailing edge of the clock signal Dckpt_d distributed to the input latch circuits 444 to 447 are controlled to be located at the center of the high-level period (one period of the clock CK0 of the block at the transmitting end) of the receiving clock Dckpt, i.e. at the center between the changing points of the data transmitted from the main circuit block PB to the subsidiary circuit block CB.

Please replace the paragraph at page 34, line 19 – page 35, line 10 with the following amended paragraph:

The gate width Wp and the gate length Lp of the p-channel MOSFET and the gate width Wn and the gate length Ln of the n-channel MOSFET are such that, in Fig. 12C showing a layout of the p-channel MOSFET Qp and the n-channel MOSFET Qn, the width of the polysilicon gate electrode PG of the p-channel MOSFET Qp is given as Lp and the length of the crossing between the polysilicon gate electrode PG and the diffusion region PSD constituting the source-drain region

of the p-channel MOSFET Qp is given as Wp. Also, in Fig. 12C, the width of the polysilicon gate electrode NG of the n-channel MOSFET Qn is assumed to be Ln, and the length of the crossing between the polysilicon gate electrode NG and the diffusion region NSD constituting the source-drain region of the n-channel MOSFET Qn is assumed to be Wn. Character LVD designates a power supply wiring conductor for supplying a source voltage ~~VDD~~Vdd, and character LVS a power supply wiring conductor for supplying a source voltage ~~VSS~~Vss.